Hasan Baig

• Engineer • Researcher • Embedded Systems Developer • Hardware / Software Developer
• Lecturer / Instructor • LabVIEW / Java Developer

Address: Building 322, Room 113, DTU, Lyngby, Denmark
Email: hasan.baig@hotmail.com
Phone: (+45) 50 34 64 53
Skype: hasan.baig
Website: www.hasanbaig.com
LinkedIn: dk.linkedin.com/in/hasanbaig

An electronic and computer engineer with a doctorate degree in computer science, having 7+ years of academic research, 1+ years of teaching, and total 3 years of industrial experiences. For details, please scroll down.

Education

- **PhD (Computer Science)** — *Aug.'14 – Oct.'17*
  Technical University of Denmark (DTU), Denmark
  Supervisor: Jan Madsen
  Examiners: Chris J. Myers (University of Utah), Swapnil Bhatia (Boston University), Michael R. Hansen (DTU)
- **MS (Computer Engineering)** – (4.4/4.5 GPA, 4.5 is best) — *Sept.'10 – Aug.'12*
  Chosun University, South Korea
- **BE (Electronic Engineering)** – (3.7/4.0 GPA, 4.0 is best) — *Jan.'06 – Jan.'10*
  NED University of Engineering & Technology, Pakistan

Professional Experience

Current Position

- **Research Assistant**, Section of Embedded Systems Engineering, *Technical University of Denmark, Denmark* – Working on the development of bio design automation (BDA) tools — *Aug.'17 - present*

Academic Research Experience

- **PhD Research Candidate**, Section of Embedded Systems Engineering, *Technical University of Denmark, Denmark* – Developed methods, algorithms, and tools for the simulation and analysis of genetic logic circuits — *Aug.'14 – Aug.'17*
- **Research Assistant**, *Chosun University, South Korea* – Worked on self-aware embedded systems — *Sept.'13 – Jul.'14*
- **Part-time Researcher**, Computer Science Department, *Umm Al-Qura University, Saudi Arabia* – Worked on the development of Wireless Sensor Motes on TI mixed signal processor MSP430. Also, developed an embedded system for "Remote Monitoring and Management System for Waste-Bins". — *Sept.'12 – Aug.'13*
- **Research Assistant**, *Chosun University, South Korea* – Worked on reconfigurable embedded systems, specifically on self-healing fault-tolerant FPGA architectures and on-chip thermal sensing through partial reconfiguration — *Sept.'10 – June'12*

Teaching Experience

- **Teaching Assistant,** Department of Applied Mathematics and Computer Science, *Technical University of Denmark, Denmark* – Served as a TA in the course entitled "Distributed Systems" — *Mar.'15 – May'16*
- **Lecturer**, Department of Computer Science, *Umm Al-Qura University, Makkah, Saudi Arabia* – Conducted undergraduate lectures for the course "Computer Organization and Assembly Language" — *Sept.'12 – Aug.'13*
- **Instructor**, Skilltech International, *Karachi, Pakistan* – Conducted a two-months course entitled "*Virtual Instrumentation"* — *June'10 – Jul.'10*

Beside above teaching experiences, I have voluntarily conducted several hands-on training workshops in different universities. The details can be seen at http://www.hasanbaig.com/conducted-workshops.

Industrial Experience

- **Internee,** Junsung E&R, Inc., *Gwangju, South Korea* — *Dec.'11 – Feb.'12*
- **Internee,** Junsung E&R, Inc., *Gwangju, South Korea* — *June'11 – Aug.'11*
- **Hardware Engineer**, EONSIL, *Karachi, Pakistan* – Developed APIs to test the Nand-flash controller for R/W operations on Nand-flash SSD. — *June'10 – Aug.'10*
- **Digital Design Engineer,** SPOT Pvt. Ltd., *Islamabad, Pakistan* – Worked on embedded image acquisition; developed different softwares on LabVIEW platform for remote fuel monitoring for Telenor and Mobilink base stations; developed TCP/IP based GPS communication software, etc. — *Mar.'10 – May'10*
- **Internee**, EONSIL**,** *Karachi, Pakistan* – Worked on embedded data storage applications and designed a dual channel nand-flash based SSD daughter card (compatible with XILINX Spartan 3A board) for testing purpose. — *Feb.'08 – Nov.'09*
- **Consultant**, EONSIL, *Austin TX, USA* – Circuit and PCB layout designing of dual-channel ONFI compatible Solid State Drive. — *June 2009*

Selected Freelance Projects	• **Tunnel Cable Automatic Fling Monitoring System**, *Junsung E&R Inc., South Korea* – Developed a Human Machine Interface (HMI) on LabVIEW platform to control and monitor the cable fling system.	*August 2011*
	• **Micro-Viscometer,** *Junsung E&R Inc. South Korea* – Developed Human Machine Interface (HMI), on LabVIEW platform, of world's first Micro-Viscometer biomedical instrument to measure blood/PBS viscosity for disease identification	*July 2011*

Selected Projects (*Complete list of projects and details can be found at http://www.hasanbaig.com/academic-research)*

• **Methods and Tools for the Analysis, Verification and Synthesis of Genetic Logic Circuits –** *Different tools and methods have been developed for simulation, timing and logic analysis, and synthesis of genetic circuits*	*PhD Thesis*
• **A self-Repairing Bio-Inspired Fault-Tolerant FPGA Architecture –** *A complete fault-tolerant FPGA architecture with self-repairing capabilities is developed and tested on XILINX XUPV5 board.*	*MS Thesis*
• **A Novel Automated Experimental Approach for the Measurement of On-Chip Speed Variations through Dynamic Partial Reconfiguration –** *A complete automated experimental setup is developed for the measurement of on-chip speed variations through dynamic partial reconfiguration. The experiment is performed on two same Virtex-5 FPGA devices based on which the intra-die and inter-die speed comparisons were made*	*Jan.'11 – July'11*
• **Performance Evaluation of CPU-GPU and CPU-only Algorithms for Detecting Defective Tablets through Morphological Imaging Techniques –** *Speed-up the image analysis time for detecting defective tablets on NVIDIA GTX 260 GPU*	*Sept.'11 – Dec.'11*
• **Development and Verification of Soft IP Core of USB 3.0 Device in Verilog HDL,** under the supervision of EONSIL, Austin TX, USA **–** *Developed a MAC Layer & Master Controller of USB 3.0 device in verilog HDL*	*BE Thesis*
• **Development of Solid State Drive** - *Designed dual-channel 8-Nand Flashes data storage device, under the supervision of EONSIL, Austin TX, USA*	*Jan.'08 – July'09*
• **Implementation of SCADA System for Unsought Tablets Detection through Morphological Image Processing –** *Developed an optimum solution for pharmaceutical industries to sort defective tablets*	*Jan.'08 – Aug.'08*

Patents

International	**Self-Repairing Fault-Tolerant FPGA Computation Unit and Architecture** *US Patent 9720766*	*Issued on Aug. 01'17*
Domestic	1. **Bio-inspired Fault-Tolerant FPGA Computation Unit** *Korea Registration Number 101279999*	*Issued on June 24'13*
	2. **Self-Repairing Bio-Inspired Fault-Tolerant FPGA** *Korea Registration Number 101400809*	*Issued on May 22'14*

Selected Research Publications / Presentations *(Complete list can be found at http://www.hasanbaig.com/patents-publications)*

Journals

1. **Hasan Baig** and Jan Madsen, "GeneTech: A Technology Mapping Tool for Genetic Logic Circuits". (*submitted to IEEE Transactions on Biomedical Engineering*).
2. **Hasan Baig** and Jan Madsen, "An Automated Approach to Verify the Logic of Genetic Circuits from Experimental Data". (*submitted to ACM Journal on Emerging Technologies*).
3. **Hasan Baig** and Jan Madsen, "A Simulation Approach for Timing Analysis of Genetic Logic Circuits", *ACS Synthetic Biology*, January 19, 2017.
4. **Hasan Baig** and Jan Madsen, "D-VASim – An Interactive Virtual Laboratory Environment for the Simulation and Analysis of Genetic Circuits", *Bioinformatics*, September 11, 2016.
5. **Hasan Baig**, Jeong-A Lee, Zahid Ali, "A Low-overhead Multiple-SEU Mitigation Approach for SRAM-based FPGAs with Increased Reliability", *IEEE Trans. on Nuclear Science*, May 2014.

Proceedings (Conference/Workshop)

1. **Hasan Baig** and Jan Madsen, "Taming Living Logic using Formal Methods", Methods, Algorithms, Logics and Tools, Lecture Notes in Computer Science (LNCS), vol. 10460, Springer, 2017.
2. **Hasan Baig** and Jan Madsen, "A Top-down Approach to Genetic Circuit Synthesis and Optimized Technology Mapping", 9th IWBDA 2017, *Pittsburgh, PI, USA*, August 08-11, 2017.
3. **Hasan Baig** and Jan Madsen, "Logic Analysis and Verification of n-input Genetic Logic Circuits", *Design Automation and Test in Europe (DATE), Lausanne, Switzerland*, March 27-31, 2017.
4. **Hasan Baig** and Jan Madsen, "Logic and Timing Analysis of Genetic Logic Circuits using D-VASim", 8th IWBDA 2016, *Newcastle upon Tyne, UK*, August 15-18, 2016.
5. **Hasan Baig** and Jan Madsen, "D-VASim: Dynamic Virtual Analyzer and Simulator for Genetic Circuits", 7th IWBDA 2015, *Seattle Washington, USA*, Aug 19-21, 2015.
6. **Hasan Baig** and Jeong-A Lee, "An Island-style-routing Compatible Fault-Tolernat FPGA Architecture with

Self-Repairing Capabilities", *FPT 2012, Seoul, South Korea,* December 10-12, 2012.

7. **Hasan Baig,** Jeong-Gun Lee and Jeong-A Lee, "A Novel Automated Experimental Approach for the Measurement of On-Chip Speed Variations through Dynamic Partial Reconfiguration", *Advances in Automation and Robotics, LNEE, Springer*, 2011, *Dubai, UAE,* December 1-2, 2011.
8. **Hasan Baig** and Jeong-A Lee, "Implementation and Functional Verification of Soft IP Core of USB 3.0 Device MAC Layer", *Proceedings of the International Conference on Embedded Systems and Applications (ESA'11), Las Vegas, Nevada, USA,* July 18-21, 2011.

Posters and Project Demonstrations

1. **Hasan Baig** and Jan Madsen, "Timing Analysis of Genetic Logic Circuits using D-VASim" in the *University Booth at DATE 2016*, Germany, March 15-18, 2016.
2. **Hasan Baig** and Jeong-A Lee, "A Novel Run-time Auto-reconfigurable FPGA Architecture for Fast Fault Recovery with Backward Compatibility", *FPGA'13 Proceedings of the ACM/SIGDA International Symposium on FPGAs, pp 270*, ISBN: 978-1-4503-1887-7, Monterey, California USA, February 12, 2013.
3. **Hasan Baig** and Jeong-A Lee, "A self-repairing Bio-inspired Fault-tolerant FPGA Architecture" in *25th ACM SIGDA University Booth and ACM SRC at 49th Design Automation Conference*, USA, Jun 3-7, 2012.

Skills and Abilities

EDA Tools

ModelSim, Xilinx tools set, OrCAD, Proteus, Electronics Workbench, NI Multisim, Code Warrior, PCB 123.

Programming Skills

C/C++, JAVA, Verilog HDL, LabVIEW, NVIDIA CUDA C, MATLAB.

Hardware

Xilinx FPGAs, NVIDIA GPU, PIC Microcontrollers, TI MSP, Arduino platform, ARM Processors (Intel XScale PXA255), NI PXI-6229, NI 9201, NI SCXI-1112, 1162, 1124 and NI cRIO-9024.

Miscellaneous

MS Office, MS Project, Adobe Photoshop, Adobe Premiere Pro, LaTeX.

Operating Systems

Windows and Macintosh

Languages

English, Urdu, Korean (Intermediate).

Awards and Honors

- Awarded a scholarship for doctoral studies and research, Denmark — *Aug.'14 – Aug.'17*
- Offered NUST faculty development program scholarship, Pakistan — *July'14*
- Offered fully funded PhD research fellowship at University of Oslo, Norway — *July'14*
- Awarded the Korean Global IT Scholarship for MS studies, *South Korea* — *Sept.'10 – Aug.'12*
- Awarded travelling grants, by Microsoft Research, to participate in ACM Student Research Competition (SRC), SF, *USA* — *June 3-7, 2012*
- Awarded traveling and living funds, by Bio-Design Automation Consortium (BDAC), to give oral talks in IWBDA consecutively for years 2015 to 2017 — *Aug. 16-18, 2015*
- Awarded travelling and living funds to present a research paper in ICFPT'12, *Seoul, South Korea* — *Dec. 10-12,2012*
- Awarded travelling and living funds to present a research paper in ICAR 2011, *Dubai, United Arab Emirates* — *Dec. 1-2, 2011*
- Given a 'Letter of Gratitude', by students' branch IEEE at NEDUET, for conducting a voluntary workshop on LabVIEW, *Karachi, Pakistan* — *March 07, 2009*

Extra-Curricular Activities

- Served as a reviewer in the Oxford journal of Bioinformatics — *April - June 2016*
- Served as a reviewer in the journal of IEEE Transactions on Nuclear Sciences — *June 2014*
- Served as a reviewing committee member in IEEE international conferences CISTI'2012 Spain, ICCCE'12 and ICIAS12 Malaysia — *Feb.'12 – Apr.'12*
- Supervised Bachelor's Thesis "An Effective Secure Novel Approach of Vehicle Monitoring by Introducing Image Capturing Module and Google Mapping" — *Jan.'11 – Dec.'11*

References

Kindly send me an email to get the contact information of referees.